REMARKS

Claims 1-36 are pending. Claims 1, 10, 16, and 25 are in independent form.

In the action mailed May 31, 2006, the title of the specification was objected to as not being descriptive. The title has been amended to address the Examiner's concerns.

Claims 1-2, 13-15, 16-17, and 28-30 were rejected under 35 U.S.C. § 112, second paragraph as being indefinite. The claims have been amended to address the Examiner's concerns.

CLAIM 1

Shoff: Claim 1 was rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent Publication No. 2005/0213377 to Shoff et al. (hereinafter "Shoff").

As amended, claim 1 relates to a data processing system. The data processing system includes a memory mapped non-volatile memory region including one or more memory mapped executable instructions to initialize the data processing system, a non-memory mapped non-volatile memory region, the non-memory mapped non-volatile memory region including one or more non-memory mapped executable instructions to initialize the data processing system, and a third memory region in communication with at least one of the memory mapped non-volatile memory region and the non-memory mapped non-volatile memory region.

The rejections contend that Shoff's NVRAM 32 constitutes a non-memory mapped non-volatile memory region that includes executable instructions to initialize a data processing system. Applicant respectfully disagrees.

In this regard, Shoff describes a compressed file system that is to be used with NVRAM. *See, e.g., Shoff*, para. [0002]. In this compressed file system, a virtual sector table (VST) maps virtual sectors to at least one physical subsector and a Sector Allocation Table (SAT) maps physical subsectors to the VST. *See, e.g., Shoff*, para. [0009]. Shoff's FIG. 3 illustrates how a sector write request from the file system is routed through the VST and the data buffer is compressed and stored in a compressed block of NVRAM 32. *See, e.g., Shoff*, FIG. 3, para. [0049]. Read operations are similarly understood to pass through the VST. *See, e.g., Shoff*, FIG. 3, para. [0055].

Schoff explicitly identifies that both the Sector Allocation Table (SAT) and the virtual sector table (VST) are generated during boot-up. *See, e.g., Schoff*, para. [0039] ("Group IDs 108 are stored in compressed subsectors to allow for generation of SAT 36 at boot-up/init time."); para. [0042] ("… VST 38 is generated on the fly from this information at boot time …").

Nothing in Shoff describes or suggests that NVRAM 32 includes executable instructions to initialize a data processing system. Instead, such instructions appear to be exclusively stored on Shoff's ROM 30. Indeed, since Shoff describes that the SAT and VST are used to access NVRAM 32 and that the SAT and VST are first generated during boot-up, it would seem illogical to contend that NVRAM 32 includes executable instructions to initialize a data processing system. For example, it would seem inefficient to require that the SAT and VST be generated before executable instructions to initialize a data processing system can be accessed.

Accordingly, claim 1 is not anticipated by Shoff. Applicant requests that the rejections of claim 1 and the claims dependent therefrom be withdrawn.

Sinclair: Claim 1 was also rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,711,059 to Sinclair et al. (hereinafter "Sinclair").

The rejection is based on the contention that Sinclair's flash memory 24 includes a memory mapped non-volatile memory region that includes executable instructions to initialize a data processing system. Applicant respectfully disagrees.

In this regard, Sinclair describes a memory controller. *See, e.g., Sinclair*, col. 1, line 13-17. A microprocessor within a memory controller can use firmware code in SRAM 12 to allow the controller to manage a storage medium to emulate a

disc memory, i.e., to create the logical characteristics of a magnetic disk device for a host. *See, e.g., Sinclair*, col. 1, line 24-29; col. 2, line 7-11.

Sinclair's memory controller 10 can operate in three different modes, one of which is an initialization/ configuration mode. *See, e.g., Sinclair*, col. 5, line 7-10. The purpose of the configuration mode is to establish the configuration information for the controller hardware and to load one or more sectors of boot firmware code to SRAM 12 of controller 10 from Flash memory 24. *See, e.g., Sinclair*, col. 5, line 27-30. *Sinclair gives no indication that memory controller 10 operates on code from Flash memory 24 during configuration*. Moreover, it appears that the boot firmware code in SRAM 12 is not memory mapped. For example, Sinclair's memory controller 10 includes a memory access control unit 14 that translates addresses generated by the memory controller microprocessor into addresses for SRAM 12. *See, e.g., Sinclair*, col. 3, line 54-55, 59-62.

Since Sinclair's memory controller 10 appears to execute boot firmware code exclusively from SRAM 12 during configuration, Applicant submits that there is no reason to believe that Sinclair's flash memory 24 includes a memory mapped non-volatile memory region that includes executable instructions to initialize a data processing system, as recited in claim 1.

Accordingly, claim 1 is not anticipated by Sinclair. Applicant requests that the rejections of claim 1 and the claims dependent therefrom be withdrawn.

Utsumi: Claim 1 was also rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,748,527 to Utsumi et al. (hereinafter "Utsumi").

The rejection is based on the contention that Utsumi's ROM 9 of FIG. 2 constitutes a non-memory mapped non-volatile memory region that includes one or more additional executable instructions to initialize a data processing system.

Applicant respectfully disagrees. In this regard, Utsumi describes a processor 10 in which the memory address of an initialization program command is generated by a fetch command control section 1 and issued to a cache unit 3 as a command address "ia." *See Utsumi*, col. 4, line 41-46. If there is a cache hit, the cache unit 3 supplies the data from the cache memory. *See Utsumi*, col. 4, line 58-61. If there is a cache miss, the cache unit 3 supplies a request address "add" to a bus control section 4 that reads data from one of RAM 6 or ROM 9. *See Utsumi*, col. 4, line 61-67.

It appears that the command address "ia" issued by fetch command control section 1 is memory mapped to Utsumi's ROM 9. For example, when Utsumi's system is powered on, one fixed value "0xFF00__0000" indicating the top address of the address area of the ROM 9 is selected. *See Utsumi*, col. 7, line 36-40; FIG. 2.

Utsumi thus neither describes nor suggests a non-memory mapped non-volatile memory region that includes one or more additional executable instructions to initialize a data processing system, as recited in claim 1. Accordingly, claim 1 is not anticipated by Utsumi. Applicant requests that the rejections of claim 1 and the claims dependent therefrom be withdrawn.

CLAIM 16

Claim 16 was rejected under 35 U.S.C. § 102(e) as anticipated by Utsumi.

Claim 16 relates to a chipset that includes a memory mapped non-volatile memory region in including one or more memory mapped executable instructions to initialize the data processing system, a non-memory mapped non-volatile memory region, the non-memory mapped non-volatile memory region including one or more non-memory mapped executable instructions to initialize the data processing system, and a third memory region in communication with at least one of the memory mapped non-volatile memory region and the non-memory mapped non-volatile memory region.

The rejection is based on the contention that Utsumi's ROM 9 of FIG. 2 constitutes a non-memory mapped non-volatile memory region that includes one or more additional executable instructions to initialize a data processing system.

Applicant respectfully disagrees. As discussed above, command addresses issued by Utsumi's fetch command control section 1 are clearly memory mapped to ROM 9. Accordingly, claim 16 is not anticipated by Utsumi. Applicant requests that the rejections of claim 16 and the claims dependent therefrom be withdrawn.

CLAIMS 10 and 25

Claims 10 and 25 were rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,601,167 to Gibson et al. (hereinafter "Gibson").

As amended, claim 10 relates to a method of initializing a computer system. The method includes (a) accessing memory mapped firmware using a processor memory read, (b) executing an initialization instruction included in the memory mapped firmware, (c) copying a page including a second initialization instruction from non-memory mapped firmware to a second memory region, (d) translating an address in the second initialization instruction to a physical address of the copied page in the second memory region, and (e) executing the second initialization instruction.

Claim 25 relates to an article of manufacture comprising a machine accessible medium containing code having instructions that, when executed, cause the machine to perform operations comparable to the method recited in claim 10.

The rejection is based on the contention that the instructions stored in Gibson's sequential access memory constitute "non-memory mapped firmware."

Without conceding the truthfulness of this contention, claims 10 and 25 have been amended to recite that an address in an initialization instruction from non-memory mapped firmware is translated to a physical address of a copied page that includes the initialization instruction in the second memory region. Such a translation is believed to be self evident from, e.g., the discussion of translation lookaside buffers and page tables in para. [0012] and from the gist of the specification as a whole.

It is clear that Gibson does not perform such a translation. Indeed, Gibson explicitly states that boot code addresses presented by Gibson's processor are ignored by the memory. *See Gibson*, col. 4, line 23-25. See also Gibson, col. 4, line 37-40 (describing that "[t]he actual address used is not critical, since the UltraNAND device will simply deliver a sequential stream of instructions that is independent of the address bus.").

Accordingly, claims 10 and 25 are not anticipated by Gibson. Applicant requests that the rejections of claims 10, 25, and the claims dependent therefrom be withdrawn.

Applicant asks that all claims be allowed. A check for the excess claim fees is enclosed. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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